ABSTRACT OF THE DISCLOSURE

In one embodiment of the invention, a processor state of a processor is determined upon expiration of a system management interrupt (SMI) timer. The processor state is one of an operational state and a low power state. The SMI timer is loaded with a timer value based on the processor state. The timer value is one of a first value and a second value. The processor is transitioned to one of the operational state and the low power state according to the processor state.